	L #	Hits	Search Text	DBs	Time Stamp
1	L1	687	(polish or polishing or cmp or chemical adj mechanical adj polishing) and pad and (passivat$6 or dielectric or inter adj layer or interlayer) and via and (tab or tape adj automated adj bonding)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:20
2	L2	83	photo and polymer and bonding adj pad and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:27
3	L3	2172	polybenzoxazole	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:20
4	L4	0	1 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:21

	L #	Hits	Search Text	DBs	Time Stamp
5	L5	2172	polybenzoxazole	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:21
6	L6	23	spin adj coat and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:21
7	L7	409	(transistor or ic or integrated adj circuit) and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:21
8	L8	34	(sribe or street) and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:22
9	L9	0	("2004/0038448").URPN.	USPAT	2005/04/14 09:25

	L #	Hits	Search Text	DBs	Time Stamp
10	L10	768	(438/459).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:25
11	L11	3	10 and 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:25
12	L12	0	photo and polymer and bonding adj pad and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:27
13	L13	1	polymer and bonding adj pad and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:27

	L #	Hits	Search Text	DBs	Time Stamp
14	L14	2	bonding adj pad and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:27
15	L15	2	bond$6 near pad and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:29
16	L16	2975	(438/106).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:28
17	L17	813	bond$6 near pad and 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:29

	L #	Hits	Search Text	DBs	Time Stamp
18	L18	2	17 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:30
19	L19	6	(("20020185721") or ("20020148733") or ("20020020855")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/14 09:31

US-PAT-NO: 6836579

DOCUMENT-IDENTIFIER: US 6836579 B2

TITLE: Surface optical device apparatus, method of fabricating the same, and apparatus using the same

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Brief Summary Text - BSTX (7):

As an example of the former method, there exists, as disclosed in Japanese Patent Application Laid-Open No. 9(1997)-223848, a method in which an epitaxial growth surface of a laser radiating layer is bonded to a Si-IC **via** a polyimide adhesive, and a GaAs growth substrate, on which the laser radiating layer had been grown, is removed by etching to obtain a surface emitting laser. FIG. 1 illustrates a cross section of this structure. An electrode of the surface emitting laser 100B fabricated by the above process is connected to an electrode 200A on the Si-IC substrate 200 **via** electrical wiring 400. Another electrode 100D is connected to a wiring pattern formed on the insulating layer 300 of polyimide. In such a structure, no alignment is needed between the optical device and the Si-IC. Further, additional processing, such as photolithography, can be conducted even after the integration, since only a functional layer of the optical device without its growth substrate is arranged on the Si and a step of the surface is hence small (about 5 .mu.m). In FIG. 1, a light receiving device 100A, an electrode 100C of the device 100A and a layer 1000 of optical devices are illustrated as well.

Brief Summary Text - BSTX (23):

The present invention is further directed to a multi-layer optoelectronic multi-chip module (MCM) including a plurality of optoelectronic multi-chip

formed by surface processing such as **via** photolithography. Accordingly, there is no need to employ a wire bonding which is inferior in yield, compactness and speed of signal transmission to the electrical wiring described above.

Detailed Description Text - DETX (22):

The substrate 30 is removed by etching in the above-described process, but the substrate 30 can also be thinned by etching and **polishing, or by polishing** only. The GaAs substrate 30 is polished to a thickness of about 1 .mu.m by **chemical mechanical polishing (CMP)**, for example, and the electrode 9 is formed on the polished surface. In this case, the above-mentioned AlAs etching stop layer and the GaAs contact layer need not be formed, and the n-side electrode 9 can be formed directly on the surface of the thinned GaAs substrate 30.

Detailed Description Text - DETX (23):

A **tape automated bonding (TAB)** tape can be used, making the above-described process of the electrical wiring unnecessary. More specifically, electrical wiring is formed on a thin film substrate, such as a polyimide film, and an electrode **pad** is formed at an area, where electrical contact with the electrode 9 of the laser is needed, on a surface of the thin film substrate opposite to its surface containing the electrical wiring, by a through-hole. The electrode **pad** is then aligned with and bonded to the electrode 9 of the surface emitting laser. The structure as illustrated in FIGS. 4A and 4B is thus fabricated. In such case, a hole is formed in the polyimide film for a translucent window.

Detailed Description Text - DETX (45):

A Si substrate 100 with an insulating layer formed on its surface is used as a base substrate. A Si-IC bare chip 106 and a surface emitting laser 104 are implemented on the substrate 100 as in the first embodiment, as a first-stage

layer. The entire surface is covered with an insulating material 101 to flatten the surface. Contact holes for electrical wiring are then formed, and electrode material 103 is used to fill in these holes. Electrical wiring 102 is formed on the insulating layer 101. Herein, only the functional layer (a thickness of about 5 .mu.m) of the surface emitting laser 104 with the GaAs substrate removed is implemented, as in the first embodiment. Corresponding thereto, the Si-IC 106 is thinned to about 5 .mu.m by **CMP**, and implemented. In such case, the following implementation may be conducted. The surface of the Si-IC 106 is set upward, the Si substrate is thinned by **polishing**, and the polished surface is then die-bonded to the substrate 100. The contact is thus electrically connected to the electrical wiring 102 through the filled electrode material 103.

Detailed Description Text - DETX (46):

When the Si-IC 106 is flip-chip implemented with its electrode surface set downward, **CMP** can be collectively performed in a state wherein the Si-IC 106 and the surface emitting laser 104 are implemented.

Detailed Description Text - DETX (47):

Second-stage and third-stage layers are similarly formed. Here, the structure is stacked after an **inter-layer** insulating layer 107 is formed. Polyimide, PSG, or the like is usually used as the insulating layer 107, but an alamido resin may also be used to make the thermal expansion coefficients closer to each other. In the second-stage layer, a light receiving device 105 is implemented, and this device 105 receives optical signals from the surface emitting laser 104 in the first-stage layer. Thus, signal connection between layers of the multi-layer wiring is achieved using light. At the same time, electrical **inter-layer** connection can also be employed using the downward

protruding electrode 103, as is illustrated in an upper portion (between the second layer and the third layer) of FIG. 12. In this case, the optical connection is preferably used at portions where high-speed transmission or **inter-layer** insulation is required.

Detailed Description Text - DETX (50):
A surface emitting laser 111, a light receiving device 112 and a Si-IC 113 are implemented on an AlN film 110 (a thin layer of resin containing AlN), for example, as in the first embodiment. The surface is flattened by a coverage with an insulating layer 114, and a wiring pattern is fabricated by forming contact holes on the surface (the wiring is omitted in FIG. 13). The wiring pattern may be formed on the AlN film 110 beforehand. The semiconductor devices 111 and 112 are thinned by **CMP** as discussed above.

Detailed Description Text - DETX (51):
Holes 116 are bored by etching, laser-abrasion, or the like, at places where an **inter-layer** connection (either optical or electrical) is needed. The electrode material is put in the hole 116 at a place where an electrical connection is needed.

Detailed Description Text - DETX (54):
After implementation is completed on each layer, the layers are stacked on the base substrate 100 and the AlN films 110 are bonded by heating and pressing. The three-dimensional MCM can be thus fabricated. Besides the AlN film 110, a film of polyimide, alamido resin, or the like may be used. Further, after each layer is implemented on a base substrate of Si, or the like, as illustrated in FIGS. 4A and 4B, each base substrate may be thinned by **polishing** and may be stacked.

Detailed Description Text - DETX (55):
The three-dimensional MCM using light for **inter-layer** connection can be

functioned as a compact high-speed electronic functional device, or as a mother
or daughter board itself which composes part of an electronic apparatus.
Further, since electromagnetic-wave noises radiated from the board can be
reduced by using optical connections, the costs of noise abatement or avoidance
can be reduced. In particular, the described MCM is effectively used in
compact portable equipment, such as portable phones, mobile equipment,
notebook-sized personal computers, digital cameras, and camera recorders.

Claims Text - CLTX (13):
13. A multi-layer optoelectronic multi-chip module comprising: (a) a
plurality of optoelectronic multi-chip modules, each said optoelectric
multi-chip module including: a surface optical device, said surface optical
device including a functional layer grown on a first substrate, which acts as a
supporting substrate for fabricating said functional layer thereon, said first
substrate being substantially thinned or removed after fabrication of said
functional layer, a first electrode formed on at least one of the surfaces of
said functional layer; and an integrated circuit for driving and controlling
said surface optical device, said integrated circuit being provided in the same
plane as the plane in which said surface optical device is provided and being
electrically connected to said surface optical device through said first
electrode; and (b) an **inter-layer** insulating layer, said insulating layer
being flattened and provided between said optoelectronic multi-chip modules,
such that the transmission and reception of an optical signal can be performed
between said optoelectronic multi-chip modules.

Claims Text - CLTX (14):
14. A multi-layer optoelectronic multi-chip module comprising: (a) a
plurality of optoelectronic multi-chip modules, each said

optoelectric
multi-chip module including: a surface optical device, said surface optical
device including a functional layer grown on a first substrate, which acts as a
supporting substrate for fabricating said functional layer thereon, said first
substrate being substantially thinned or removed after fabrication of said
functional layer, a first electrode formed on at least one of the surfaces of
said functional layer; a second substrate of an insulating thin film, said
second substrate including a second electrode formed thereon, and said surface
optical device being bonded to said second substrate, with said first electrode
and said second electrode being in electrical contact with each other; and an
integrated circuit for driving and controlling said surface optical device,
said integrated circuit being provided on said second substrate, and
electrically connected to said surface optical device through said second
electrode; and (b) an **inter-layer** insulating layer, said insulating layer
being provided between said optoelectronic multi-chip modules, such that
transmission and reception of an optical signal can be performed between said
optoelectronic multi-chip modules.

Related Application Filing Date - RLFD (1):
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